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ARMY ELECTRONICS TECHNOLOGY AND DEVICES LAB FORT MON--ETC F/G 9/1
SEMI-INSULATING GALLIUM ARSENIDE FOR MILLIMETER WAVE AND HIGH S--ETC(U)
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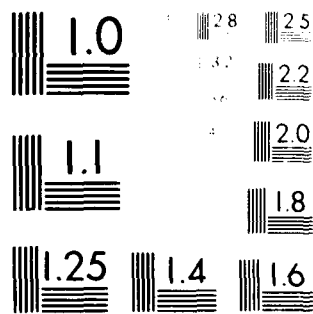
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WINTER and MALIKSEMI-INSULATING GALLIUM ARSENIDE FOR MILLIMETER
WAVE AND HIGH SPEED IC DEVICE APPLICATIONS

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INTRODUCTION

A wide variety of semiconductor devices utilizing gallium arsenide (GaAs) is currently under development by the military for use in advanced communication, surveillance, and target acquisition systems. GaAs, a compound semiconductor exhibiting a large energy bandgap, is characterized by a high intrinsic electron mobility ($8600 \text{ cm}^2\text{V}^{-1}\text{sec}^{-1}$ @ 300°K) and resistivity ($> 10^8 \text{ ohm-cm}$). The low-field electron mobility of GaAs is one of its greatest attributes and offers high frequency operation in devices such as the field effect transistor (FET). Coupled with the material's high peak velocity and low threshold field, GaAs integrated circuit (IC) devices offer a two to six time speed improvement over their silicon counterparts. When compared with standard silicon IC technology, the process steps for GaAs ICs are relatively simple and few in number. As a result of these advantages, the technology of manufacturing high performance GaAs devices is maturing at a rapid rate. Thus, it is not surprising to find these devices experiencing a greatly expanding role in oscillator, mixer, logic element, power amplification, and low noise/high gain application. However, the full potential and low-cost manufacture of GaAs devices has yet to be realized, partly due to material problems experienced by substrate suppliers and device manufacturers.

It is commonly held by major GaAs device manufacturers that the quality of semi-insulating substrates is one of the barriers to obtaining reliable, reproducible, high-performance devices. In addition, because the quality of commercially available semi-insulating GaAs substrates is highly variable, extensive material

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qualification tests are required before substrates are accepted for device fabrication. It has been shown that chromium (Cr), which is used to compensate native impurities and produce high resistivity in GaAs, redistributes during thermal processing (1-3), whether during a subsequent epitaxial process or a high temperature ion-implantation anneal procedure. Typically, the Cr depletes from a region one or two microns deep and migrates to the surface where it occupies a region about 400°\AA thick. The most serious consequence of this distribution is that the depletion of Cr can uncompensate some of the native donor impurities existing in the n-depleted region, resulting in excess uncontrolled n-type activation and significant changes in device characteristics and reliability. In addition to this "surface conversion" problem, fast diffusing deep-level acceptors, carbon-arsenic vacancy complexes and diffusing deep-level impurities are still observed as a result of process-induced substituents.

In order to minimize the effect of substrate imperfections on devices fabricated by epitaxy, one usually grows a high quality buffer layer to isolate the device from the substrate. However, the epitaxial approach has two major drawbacks; cost and difficulty in achieving the required thickness and uniformity. Although ion-implantation reduces the cost of active layer fabrication, the important properties of the implanted layers, such as mobility and doping profile, can be significantly affected by substrate characteristics. In addition, inter-device leakage becomes a problem if Cr redistribution causes a thin conducting layer to form on the GaAs surface during the high temperature implant anneal procedure.

The alternative solution to these problems is to improve the quality of substrate material through the reduction of impurity and defect levels and/or the elimination of charge compensators such as Cr. Such is the objective of our research program.

CRYSTAL GROWTH

The technology involved in the growth of GaAs is considerably more complicated than that employed for silicon, for one is dealing with more complicated binary phase equilibria and a highly volatile component, arsenic. Precise control of the As vapor pressure in the chosen growth system is required in order to maintain exact stoichiometry of the GaAs compound during the growth process so as to achieve high mobility and crystal perfection.

The bulk compound is normally formed by the reaction of As vapor with Ga metal at elevated temperatures in sealed quartz ampoules as shown in Fig. 1. Typically, an As reservoir contained at one end of

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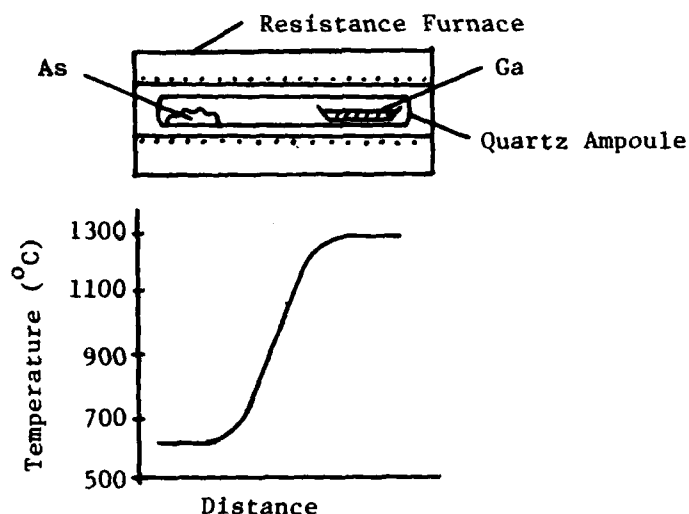


Fig. 1. Typical furnace and temperature profile for compounding GaAs in quartz.

the ampoule is heated to 600°C. This generates approximately 1 atm of As vapor pressure in the system, a prerequisite for obtaining stoichiometric GaAs (4). The As vapor reacts with the Ga metal maintained at approximately 1260°C and located at the other end of the ampoule in a quartz boat. After the Ga has been completely reacted, single crystal growth may be initiated by programmed cooling (gradient freeze) or by physically moving either the ampoule or furnace to provide proper temperature gradients for growth. This process is commonly referred to as the "horizontal Bridgeman" technique and is the method used by all major commercial GaAs material suppliers to date. Crystals prepared by this technique have a "half moon" cross-section and, therefore, result in considerable waste in IC processing where the required shape is a circular disk.

Another approach to the commercial production of bulk GaAs which is gaining favor is the liquid encapsulated Czochralski technique (LEC CZ). Metz et al (5) first described the use of an encapsulant to suppress the loss of a volatile component from a melt. Mullin et al (6) used this method for the growth of InAs and GaAs from stoichiometric melts. In this method, shown in Fig. 2, the vaporization of As from molten GaAs is inhibited by placing a layer of a non-reactive encapsulant (e.g., B₂O₃) on the melt surface. An inert gas pressure which is higher than the As vapor pressure is then maintained over the molten B₂O₃ layer. A rotating seed crystal contacting the molten GaAs is then slowly withdrawn through the liquid

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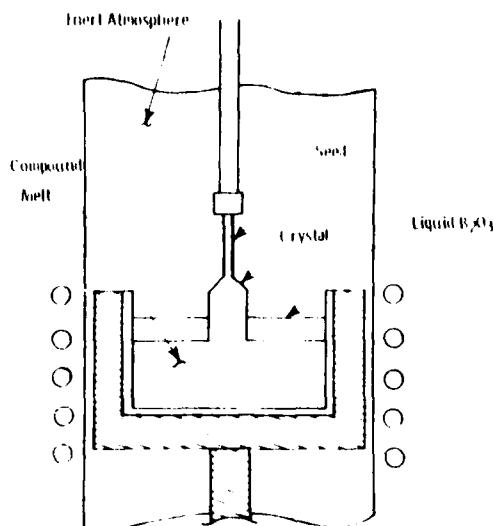


Fig. 2. Liquid encapsulated Czochralski pulling technique.

encapsulant while the temperature is regulated to obtain the desired diameter crystal. The advantage of the LRC CZ technique is the ability to prepare large diameter crystals in a relatively short period of time. However, the GaAs polycrystalline source material used in this technique and from which the crystal is pulled, is normally compounded in quartz ampoules. The use of quartz as a container for Ga, As, and molten GaAs, or as a reaction vessel can lead to appreciable silicon contamination (7). Since silicon can act as a shallow donor or acceptor in GaAs (8), chromium, a deep-level acceptor and/or oxygen, a deep-level donor, must be deliberately added in order to compensate the GaAs, thereby making it semi-insulating ($> 10^8$ ohm-cm).

A second drawback to the conventional LEC CZ technique is its separate two step process - compounding and subsequent crystal growth. Because of this increased handling, more impurities can be introduced than those obtained in the horizontal Bridgeman process. The in-situ LEC compounding/Czochralski growth process we describe for growing semi-insulating GaAs incorporates, for the first time, both steps and eliminates all dependence on quartz components, thereby, reducing or eliminating the requirement for chromium compensation. This is accomplished by reacting elemental gallium and arsenic under a molten encapsulant in pyrolytic boron nitride (PBN) crucibles at nitrogen pressures to 100 atm. A specially designed

(236)

ROSS, AUCOIN, SAVAGE
WINTER and MALIK

high pressure Czochralski crystal pulling system, Varian model HPCZ, was used for maintaining the nitrogen gas ambient and for growth of the bulk GaAs (see Fig. 3). This system contains provision for the following: rotation of the crystal and/or crucible; raising and lowering of the crystal and/or crucible; remote control of temperature, gas flow, pulling and rotation rates; TV process monitoring; cryo fore-pumping; vac-ion pumping to 10^{-5} torr; hydraulic lifting of the chamber; and is designed for operation at pressures to 135 atm with neutral, oxidizing or reducing ambients.

The in-situ LEC compounding and Czochralski growth of GaAs was carried out in the following manner. The PBN crucibles were etched in HCl, rinsed with de-ionized water following by methonal and then vacuum dried overnight at 200°C . The crucibles were then loaded with stoichiometric quantities of high-purity gallium and arsenic. A dehydrated pellet of boron oxide encapsulant was placed on top of the charge and the entire assembly centered within a tantalum or graphite susceptor in the Czochralski pulling chamber as shown in Fig. 4.

It was found that if the boron oxide encapsulant contained an excessive amount of moisture, bubbles continuously formed at the melt/encapsulant interface. These bubbles subsequently rose to the surface releasing arsenic which, in turn, led to nonstoichiometric melts and resultant twinning of the crystals. An oil-free, high-vacuum baking system was constructed to further dehydrate the pellets. Heating the boron oxide to approximately 1000°C at 10^{-7} torr in induction heated platinum/gold crucibles was found to give satisfactory results.

After the growth station was established (susceptor, crucible, gallium, arsenic, boron oxide, etc.) and the chamber closed, the system was evacuated to 10^{-5} torr. The charge was then slowly heated to 325°C to remove residual moisture and volatile gallium/arsenic oxides. If the temperature exceeded 325°C , significant amounts of arsenic were lost by volatilization prior to compounding. After several hours, the system was then backfilled with high-purity nitrogen gas to 3.0 atm and the temperature increased to 450°C . During this step, the boron oxide melted and flowed into the voids. The pressure in the pulling chamber was then increased to 60 atm. As the temperature was slowly increased, the compounding reaction could be observed on the TV monitor being accompanied by a rapid temperature rise as the crucible approached 700°C .

Single crystals of GaAs were grown from the in-situ compounded material by the LEC CZ technique as previously shown in Fig. 2. All crystals were grown in the $\langle 111 \rangle$ -B direction with nitrogen gas

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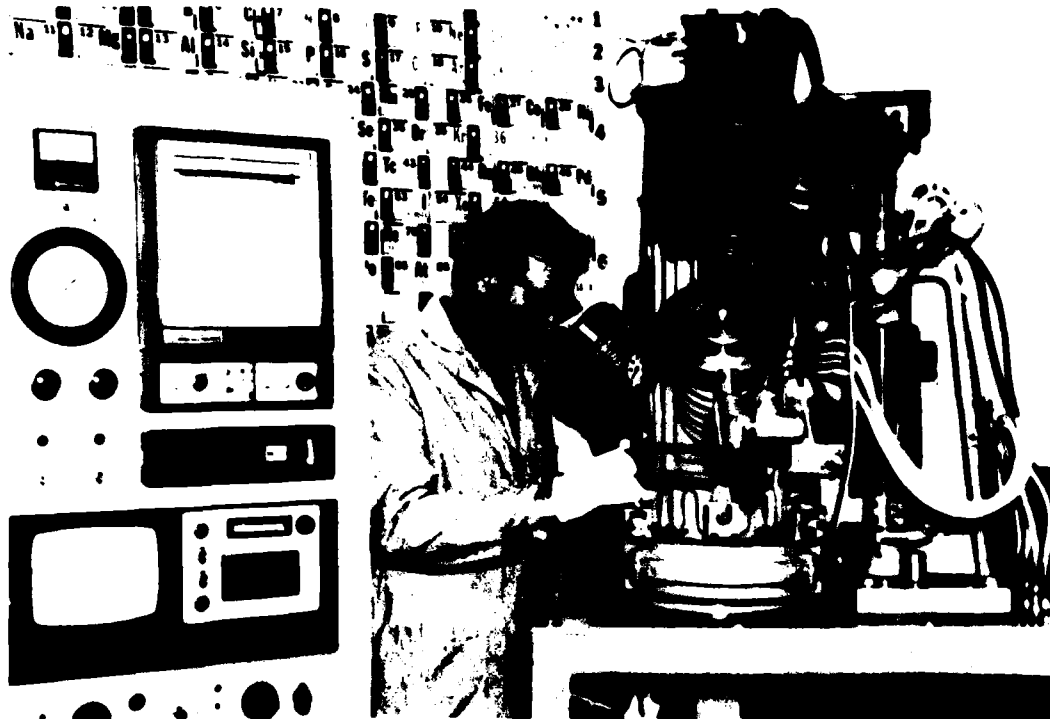


Fig. 3. High pressure Czocharalski crystal pulling system.

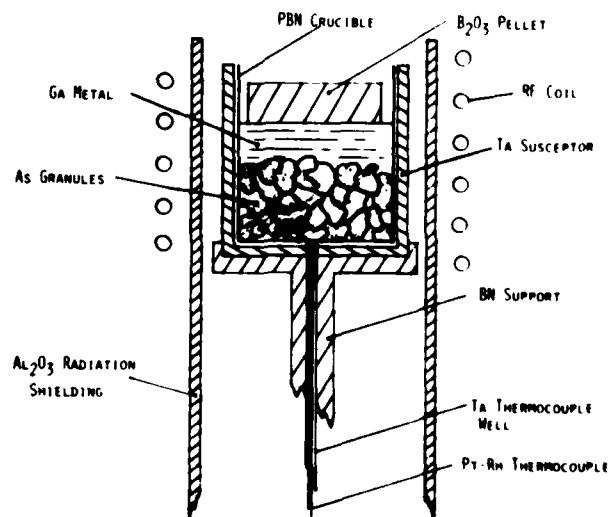


Fig. 4. Arrangement for liquid encapsulated compounding of GaAs.

ROSS, AUCOIN, SAVAGE
WINTER and MALIK

pressures of 1.0 to 20.0 atm. and pulling rates of 1.0 to 2.0 cm/hr. Both concurrent and countercurrent rotation of crucible and crystal were used at rates of 5 and 15 rpm respectively; the concurrent rotation producing a more convex interface.

ELECTRICAL MEASUREMENTS

The measurements of resistivity, Hall mobility and Hall coefficient have been performed using the van der Pauw method (9). This technique has the advantage in that only four contacts are required and only the sample thickness need be known. In this work, the conventional "clover-shaped" sample geometry is replaced by an equivalent "Greek-cross" structure (10) (see Fig. 5). The actual GaAs structures are produced using an ultra-sonic milling machine.

The resistivity, ρ , in ohm-cm is given by

$$\rho = \frac{\pi t}{\ln 2} \left[\frac{R_{AB,CD} + R_{BC,DA}}{2} \right] F$$

where $R_{AB,CD} = V_{AB}/I_{CD}$

and $R_{BC,DA} = V_{BC}/I_{DA}$

are in units of ohms, t is the sample thickness in centimeters and F is the van der Pauw factor which is a dimensionless quantity dependent only upon the ratio of $R_{AB,CD}/R_{BC,DA}$ and is defined by the transcendental equation

$$\cosh \left[\frac{\ln 2}{F} \cdot \frac{R_{AB,CD}/R_{BC,DA} - 1}{R_{AB,CD}/R_{BC,DA} + 1} \right] = \frac{1}{2} e^{\ln 2/F}$$

The Hall mobility, μ_H , in $\text{cm}^2 \text{volt}^{-1} \text{sec}^{-1}$ is given by

$$\mu_H = 10^8 \frac{t}{B \rho} \Delta R_{AC,BD}$$

where B is the applied magnetic field in gauss and $\Delta R_{AC,BD}$ is the change in resistance when the magnetic field is applied perpendicular to the sample. The Hall coefficient, R_H , in $\text{cm}^3/\text{coulomb}$ is calculated from

$$R_H = \rho \mu_H$$

The disadvantage of the van der Pauw method is that two resistances ($R_{AB,CD}$ and $R_{BC,DA}$) must be measured requiring that voltage and current leads be switched. In addition, good experimental practice dictates that current leads be reversed and switched in order to



Fig. 5. Sample geometry.

ROSS, AUCCOIN, SAVAGE
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eliminate contact resistances and potentials, rectifying effects and thermal emfs. Thus, in the collection of van der Pauw transport data, eight configurations are used for resistivity measurement (Fig. 6. (a)-(h)) and eight for mobility measurement (Fig. 6. (i)-(p)).

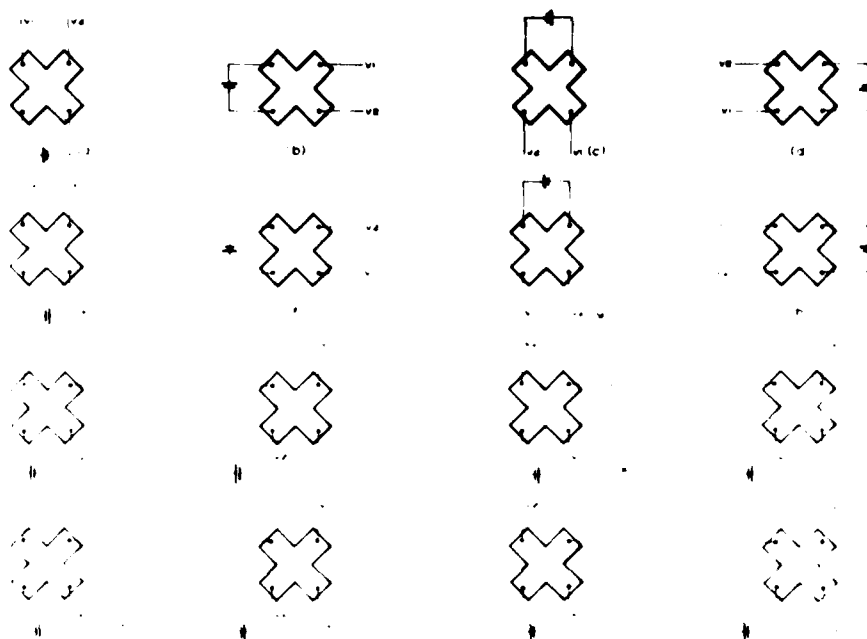


Fig. 6. SAMPLE CONFIGURATION FOR VAN DER PAUW TRANSPORT DATA

(a) - (h) RESISTIVITY
(i) - (p) MOBILITY

The switching of current and voltage leads and the reversing thereof is accomplished by the arrangement shown in Fig. 7. The sample is contained in a fully shielded and evacuated chamber (Fig. 8.) and is connected to four electrometers by triaxial cable, the inner shield of which is driven by the output of each electrometer. Shielded coaxial reed relays provide the required lead switching to generate the various circuit configurations of Fig. 6. The result is a fully guarded system capable of measuring samples having up to 10^{12} ohms resistance with a minimum of noise and settling time.

Because of the large number of measurements necessary and the large number of samples investigated, the guarded van der Pauw system of Fig. 7. was automated whereby all switching of leads and electro-

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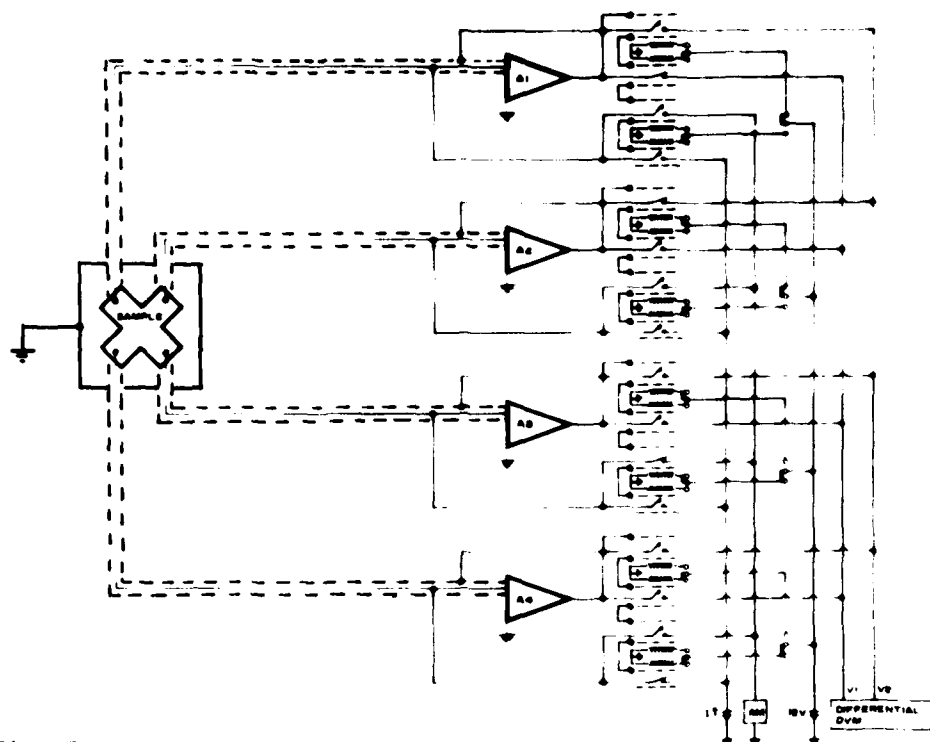


Fig. 7. GUARDED VAN DER PAUW SYSTEM

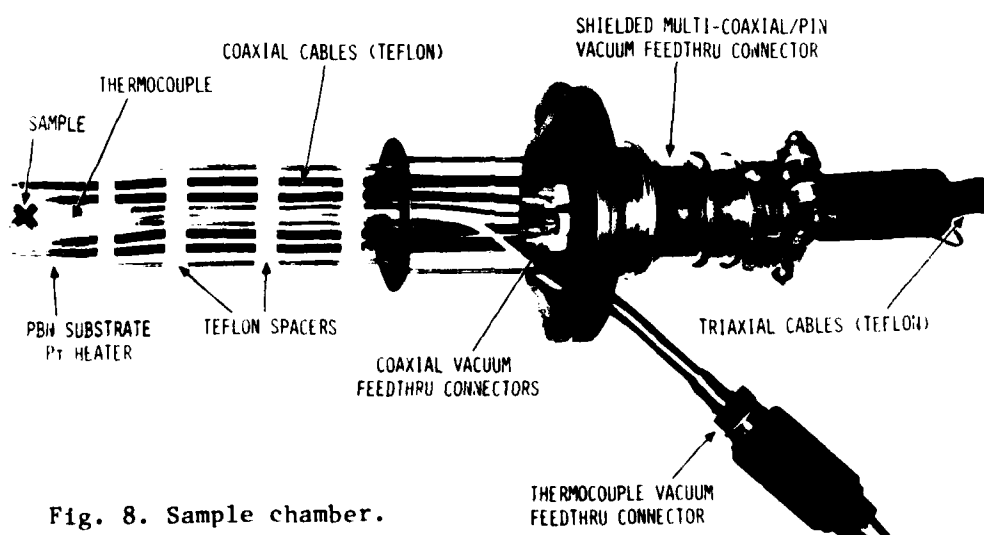


Fig. 8. Sample chamber.

(241)

ROSS, AUCOIN, SAVAGE
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meters, measurement of current and voltage and calculation of parameters is accomplished under the control of a programmable calculator (Fig. 9.). The system is presently under expansion to provide for automatic magnetic field selection and temperature control.

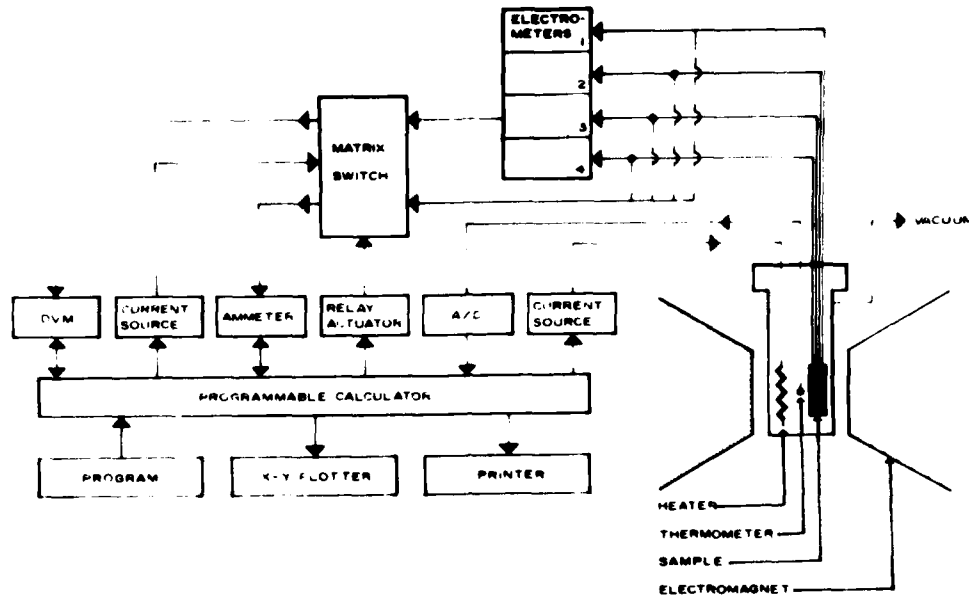


Fig. 9.

AUTOMATED VAN DER PAUW HALL AND RESISTIVITY SYSTEM

MIXED CONDUCTION ANALYSIS

When one carrier type dominates the conduction process, simple Hall coefficient and resistivity measurements at low magnetic fields provides values of carrier concentration and mobility. Semi-insulating GaAs, however, exhibits mixed conduction; i.e., conduction by both holes and electrons. This complication requires additional information, in particular, the magnetic field dependence of both Hall coefficient and resistivity, in order to permit resolution of the independent carrier properties.

The total Hall coefficient is given by

$$R = \frac{R_n \sigma_n^2 + R_p \sigma_p^2 + R_n R_p \sigma_n^2 \sigma_p^2 (R_n + R_p) B^2}{(\sigma_n + \sigma_p)^2 + \sigma_n \sigma_p (R_n + R_p)^2 B^2} \quad (1)$$

ROSS, AUCOIN, SAVAGE
WINTER and MALIK

and the total conductivity by

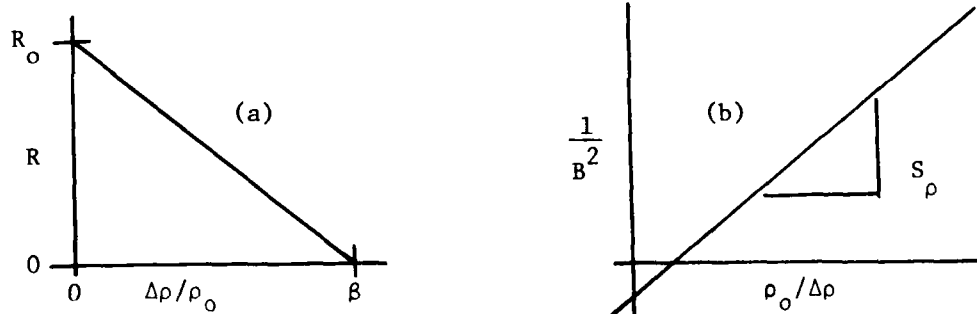
$$\sigma = \frac{(\sigma_n + \sigma_p)^2 + \sigma_n^2 \sigma_p^2 (R_n + R_p)^2 B^2}{\sigma_n (1 + R_n^2 \sigma_p^2 B^2) + \sigma_p (1 + R_p^2 \sigma_n^2 B^2)} \quad (2)$$

where the subscripts n and p indicate the contribution due to electrons and holes, respectively, and B is the magnetic field (11). Using the intermediate functions X, Y, and Z (12), equations (1) and (2) can be rewritten as

$$R = R_o \left[1 + \frac{Y + Z}{X} \frac{\Delta \rho}{\rho_o} \right] \quad (3)$$

$$\frac{1}{B^2} + \mu_n^2 Y = \mu_n^2 X \frac{\rho_o}{\Delta \rho} \quad (4)$$

where ρ_o is the resistivity at zero magnetic field, $\Delta \rho = \rho(B) - \rho_o$ and is called the magneto-resistivity and R_o is the Hall coefficient, equation (1), at zero magnetic field. Varying the magnetic field from 0 to 18kG and plotting equations (3) and (4) yields curves (a) and (b) as shown.



Curve (a) gives R_o and $\beta = X/Y+Z$ whereas curve (b) yields the slope $S_\rho = -\mu_n^2 X$. Letting:

$$T = (R_o \sigma_o)^2 / S_\rho, \quad A = [2 + T(1 + \beta^{-2})] / (1 + T/\beta)$$

$$b = [A + (A^2 - 4)^{1/2}] / 2\alpha, \quad c = (1 + \alpha b \beta) / [b(\alpha b + \beta)]$$

where $\alpha = r_n / r_p$ and is the ratio of scattering factors and assumed to be unity, then the individual carrier properties can be calculated from:

ROSS, AUCOIN, SAVAGE
WINTER and MALIK

$$\text{electron mobility} = \mu_n = \frac{1 - \beta^{-1}}{\alpha - b^{-1}} \cdot \frac{(-R_0)\sigma_0}{r_p} \text{ cm}^2 \text{ volt}^{-1} \text{ sec}^{-1},$$

$$\text{hole mobility} = \mu_p = \mu_n/b \text{ cm}^2 \text{ volt}^{-1} \text{ sec}^{-1},$$

$$\text{hole concentration} = p = \frac{\sigma_0}{q\mu_n} \cdot \frac{1}{c + b^{-1}} \text{ cm}^{-3},$$

$$\text{electron concentration} = n = cp \text{ cm}^{-3},$$

$$\text{intrinsic carrier concentration} = n_i = (np)^{1/2} \text{ cm}^{-3}.$$

In addition, the Fermi level can be calculated from

$$E_c - E_F = kT \ln(N_c/n),$$

where N_c is the effective density of states in the conduction band.

An indication of the accuracy of this mixed conduction analysis is given by the linearity of equations (3) and (4) and the similarity of the calculated value of n_i to its theoretical value of 1.5×10^6 (12).

Table 1. compares the electrical properties of undoped GaAs grown by the ET&DL process to chromium doped substrates from other sources. Although the resistivity is slightly lower, the ET&DL material has one of the highest electron mobilities, nearly equal carrier concentrations and a Fermi energy level nearly intrinsic. Recent growths have resulted in material with resistivities of 0.8×10^9 ohm-cm. In addition, thermal conversion analysis indicates the material is stable to 700°C for 30 minutes in H_2 , ultimately converting to p-type at 1000°C .

SUMMARY

The physical and electrical properties of GaAs show it to be an important semiconductor material for use in advanced military electronic systems. However, millimeter wave and high speed IC device development has been slowed due, in part, to poor and unpredictable quality semi-insulating substrate material. A new modification of the liquid encapsulated Czochralski pressure-assisted growth process has been developed which employs in-situ compounding of GaAs from its elements. This process, first demonstrated in the U.S. by ET&DL, consistently yields high resistivity (to 10^9 ohm-cm) GaAs without the intentional addition of charge compensators. Transport property

ROSS, AUCOIN, SAVAGE
WINTER and MALIK

	ρ_o	$-R_o$	μ_n	μ_p	n	p	n_i	$E_c - E_F$
	$\times 10^9$	$\times 10^3$	$\times 10^3$	$\times 10^2$	$\times 10^6$	$\times 10^6$	$\times 10^6$	
	ohm cm	cm ³ /coul	cm ² /Vsec	cm ² /Vsec	cm ⁻³	cm ⁻³	cm ⁻³	eV
HP	1.21	2.25	3.41	8.44	.963	2.23	2.76	.684
NRL	.697	1.95	5.85	8.42	.832	5.94	2.22	.688
Laser Diodes	.733	1.80	2.94	4.90	2.48	2.48	2.48	.660
Monsanto	.0645	.370	5.74	..	16.9611
Morgan	.843	.647	4.73	5.55	.392	10.0	1.98	.707
Crystal Specialties	.897	2.48	4.43	5.19	1.04	4.50	2.16	.682
Sumitomo	.961	1.14	4.40	4.21	.492	10.2	2.25	.701
ET&DL*	.420	1.67	5.37	9.89	2.16	3.33	2.68	.664

*non-Cr doped n_i (theoretical) = 1.5×10^6 cm⁻³
 $E_c - E_F$ (theoretical) = 0.675 eV

Table 1. Comparison of electrical properties of undoped GaAs (ET&DL) to chromium doped substrates from other sources.

determinations by mixed conduction analysis indicates the material has electron mobilities higher than Cr-doped material and Fermi levels which are nearly intrinsic.

The one step technique for "in-situ" liquid encapsulated compounding and Czochralski growth of GaAs is believed to be the best approach to solving the current problems associated with semi-insulating substrate fabrication. Various semiconductor material and device manufacturers such as Varian Associates, Westinghouse, Hughes, Rockwell, Microwave Associates and Metals Research are in the process of acquiring, or have purchased equipment to grow semi-insulating GaAs by this technique. Indeed, this approach is now becoming the basis for U.S. volume production of large diameter, high quality, semi-insulating GaAs material.

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245

ROSS, AUCOIN, SAVAGE
WINTER and MALIK

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